Remarks

Claims Status

The originally filed claims were 1-19. Claims 11-19 were withdrawn in response to a restriction. Claims 20-30 were added but were held to be constructively withdrawn as being directed to a non-elected invention. Claims 1-10 are remaining. To distinguish and clarify the invention, the claims 1-10 have been amended with the word "transistor" replaced by "cell" as explained below.

Appropriateness of Final Rejection

Applicant objects to the final rejection as being premature since the final rejection is based on new prior art, namely the patent to Lee et al., U.S. Pat. No. 6,687,154. The final rejection is inappropriate because the prior amendment was clarifying and did not introduce substantially new limitations. In other words, the reference could have been cited in the first Office action, but was not. Applicant did not introduce any new concepts which were not latent in the original claims. Withdrawal of the final rejection is requested.

Rejection of Claims 1-10

Claims 1-6, 9-10 are rejected under 35 U.S.C. § 102(e) as being anticipated by Lee et al. The Examiner asserts that the non-volatile memory transistors and the read only memory transistors have the same area footprint within a single memory array (col. 13, line 13-32).

In fact, lines 13-32 refer to Fig. 7B of Lee et al., which is a side view of two serially connected transistors, one of which is a memory transistor and one of which is a mask ROM transistor, acting as a select transistor. There is no top view which would show that the two transistors have the same footprint. Normally, a select transistor and a flash

memory transistor have different footprints. The fact that both devices "rely on the same process" merely means that the layers for both transistors are the same. The footprints may or may not be the same. The Examiner in inferring that because the layering process is the same, that the top view would be the same even though the transistors have different purposes, one transistor being a memory transistor and the other transistor being a select transistor.

Anticipation under 35 U.S.C. § 102(e) requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.", Verdegaal Bros. Inc. v. Union Oil Co., 814F.2.d., 628, 631, 2USPQ2d, 1051-1053 (CAFC 1987), In re Robertson, 169F3d743, 49USPQ2d 1949, (CAFC 1999), to establish inherency, "extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.'" [citation] 'inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." [citation], In re Robertson, 49USPQ2d, 1950-1952. Accordingly, the rejection is believed to be traversed.

Distinguishing Features of Amended Claims

Amended independent claim 1 recites the fact a user programmable memory cell has the same footprint as a read only memory cell. Each cell consisting of two transistors, namely a memory transistor and a select transistor. In Lee et al., all the memory cells are the same and include a memory transistor connected in series to a select transistor, as shown on the cover page of the patent and in Fig. 4, Fig. 5, Fig. 6, and Figs. 7A-7D. In all of these figures, the memory transistor and the select transistor share a common electrode, namely drain 78. And, so the transistors cannot possibly have

the same footprint because drain 78 must be allocated between the two transistors. What fraction of drain 78 will be allocated to transistor 70a? What fraction of drain 78 will be allocated to select transistor 70b? Because drain 78 is non-divisible, but shared, the two transistors cannot have the same footprint.

In addition, Applicant has amended claim 1 to recite that memory cells, both user programmable and mask programmed, have a memory transistor and a select transistor. Thus, two cells are being compared, with each cell having the same footprint and having two transistors. In the Lee reference, two transistors are being compared that are not independent of each other, but share a drain electrode and form a single memory cell. Different comparisons are being made and so an inherency rejection cannot be sustained, Verdegaal Bros. Inc. v. Union Oil Co., In re Robertson, supra.

Subject Matter of Claim 2 Incorporated in Claim 1

It should be noted that claim 2 has been cancelled. Previously, claim 2 contained the limitation that the footprint included the select transistor thus, the amendment of claim 1 incorporates the subject matter of claim 2 and so claim 1 does not go beyond the scope of subject matter which has previously been examined. No further examination of the application should be necessary if claim 2 was previously examined.

On page 4 of the Office action, regarding claim 2, the Examiner states that Lee discloses two "cells". The Examiner is mischaracterizing the Lee reference. A "cell" is a memory storage unit. A cell may have a single transistor or it may have two transistors, the latter situation where the memory transistor uses an auxiliary transistor such as a select transistor. For example, see the book "Semiconductor Memories" by A. Sharma, IEEE Press 1997, p. 107 for example of single transistor memory cell and p. 117 for a 2-transistor

cell having an EEPROM and a select transistor. The latter is Applicant's usage of "cells". See specification, p. 3, lines 26, 31; page 5, line 2. A cell with more than two transistors is also possible. In column 6, line 16, Lee refers to a "2T cell M41". This means a two transistor memory cell 41 including flash transistor M41a and mask ROM transistor 41b. Accordingly, Lee does not have "two cells" stated by the Examiner but a single two transistor cell.

Subject Matter of Claim 3

On page 5 of the Office action, regarding claim 3, the Examiner states that Lee discloses a longitudinal dimension and a width dimension that are the same for both the first and second pluralities of transistors, with the select transistor and memory transistor having a common electrode." In the first place, there is no such disclosure of what the "footprint" may be. There is no discussion of "longitudinal dimension" and "width dimension". There is certainly no statement that the two footprints are the same. Moreover, the Examiner's acknowledgment that the select transistor and the memory transistor have a common electrode proves that the two transistors cannot possibly have the same footprint since the footprints must overlap without any clear delineation where one stops and the other begins. The Examiner notes that in Fig. 4, the memory cell in the select transistor without control gate and gate [sic] are connected through lines 40a, 40b, 40c, and 40d and therefore have common electrodes. This is a connectivity which has nothing to do with footprint. The lines 40a, 40b, 40c, and 40d are word lines connecting transistors in the same row. These lines have nothing to do with "a first plurality of user programmable memory cells including a memory transistor and a select transistor and a second plurality of mask programmed read only memory cells including a memory transistor and a select transistor... having the same footprint...", set forth in claim 1.

Applicant's claim 4 relates to a programming state of the "read only memory cells having... open channels and cells having... shorted channels". This has nothing to do with word lines.

Subject Matter of Claim 4

With regard to claim 4, claim 4 is dependent on claim 1 and includes all of the limitations which applicant incorporates herein. As such, claim 4 is distinct from Lee for at least the same reason as claim 1.

Subject Matter of Claim 5

Regarding claim 5, in the non-volatile memory cells of Applicant there are two transistors, a memory transistor and a select transistor. These two transistors have two poly layers. On the other hand, the read only memory cells, also with two transistors, have only one poly layer. Since Lee is working with cells of two transistors and since Applicant is working with two cells each having two transistors, i.e., four transistors, the structures are not identical and therefore cannot be anticipated.

Subject Matter of Claim 6

With regard to claims 6, Applicant has claimed read-only memory cells grouped into rows. In Lee, there is no read-only memory cell. Rather, the cells are both the user programmable memory transistors and the auxiliary read-only memory transistors acting as select transistors.

Subject Matter of Claim 9

Regarding claim 9, mentioned at the bottom of page 5 of the Office action, it should be pointed out that Applicant's claim 9 is dependent on claim 4, in turn, dependent on claim 1. The argument made above with reference to claim 4 is applicable to claim 9.

Subject Matter of Claim 10

At the top of page 6 of the Office action, regarding claim 10, it is asserted that Lee shows non-volatile memory transistors. This is correct. Applicant relies on the patentability of claim 10 from independent claim 1 where the cells of Applicant are distinguished as different from the cells of Lee.

Section 103 Rejection of Claims 7 and 8

On page 7 of the Office action, claims 7 and 8 were rejected under 35 U.S.C. § 103(a) in view of Lee et al. Applicant disputes the claim that Lee discloses the invention of claim 8 except for the condition of programming. It has been pointed out above that the cell structure of Lee is completely different from that of Applicant and that the shared drain shown in the Lee cell prevents footprints of the two transistors from being identical without speculating on how to attribute the shared electrode. While it is true that Lee discloses ROM cells which can be programmed in two logic states, the structure of respective transistors and cells is different. Accordingly, it would not be obvious to one skilled in the art to devise Applicant's cells from the teachings of Lee since Lee teaches the programmability of a select transistor. On the other hand, Applicant does not teach the programmability of the select transistor but rather of the principal transistor in a memory cell. A person skilled in the art would be led away from Applicant's teachings when considering Lee et al.

Conclusion

Reconsideration of the claims, as amended, is requested. Applicant believes the claims traversed the rejections set forth in the Office action. A Notice of Allowance is earnestly solicited.

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signed: Sally Azevedo

Typed Name: Sally Azevedo

Date: June 9, 2006

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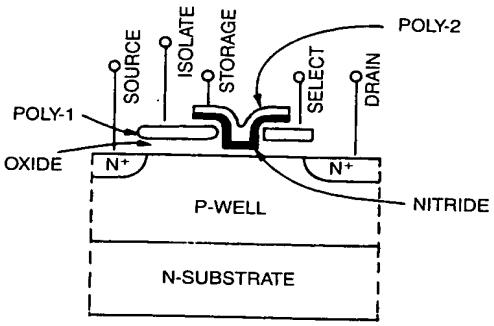
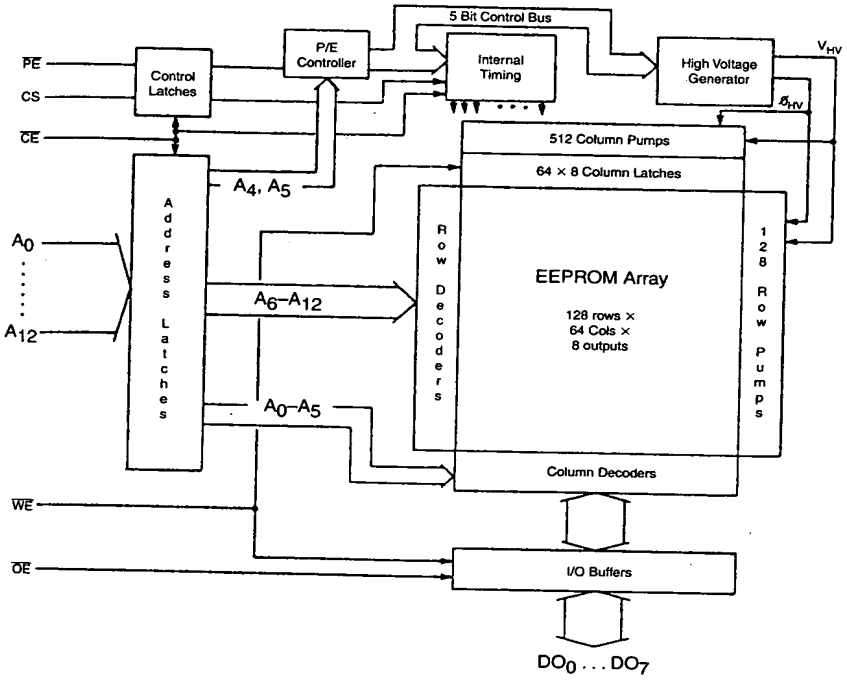


(a)



(b)

Figure 3-21. A +5 V-only Inmos EAROM. (a) Schematic cross-section. (b) Functional block diagram. (From [44], with permission of IEEE.)

...ce greater than 10^4 write/erase cycles, and ...-year data retention at 85°C. Figure 3-22(a) ...s the memory cell layout. A memory cell ...s formed in 32 wells, and each well con- ...f 8 × 256 memory cells. 8 b placed in the ...on of the word line in each well corre- ...o 1 byte, or eight sense amplifiers and eight input/output buffers. The high-voltage system for on-chip generation of programming voltage is regulated with an accuracy of ±1 V using a Zener diode formed in a p-type well. This high-voltage system and the memory cell array are shown in the functional block diagram of Figure 3-22(b).

tunneling takes place from the substrate to the floating gate. Also, the interpoly oxides through which the tunneling takes place can be significantly thicker (60–100 nm) than those for the FLOTOX devices since the electric field is enhanced by geometrical effects of fine texture at the surface of polysilicon structures.

Textured polysilicon cells are programmed by causing the electrons to tunnel from poly 1 to floating gate (poly 2), and erasure by the electron tunneling from poly 2 to poly 3. The poly 3 voltage is taken high in both the programming and erase operations. However, it is the drain voltage which determines whether the tunneling takes place from poly 1 to the floating gate, or from the floating gate to poly 3. This implies that the state of the drain voltage determines the final state of the memory cell. This has the advantage of being a "direct write cell" with no need to clear all the cells before write, as is the case with the FLOTOX-cell-based EEPROMs.

The manufacturing process for textured-polysilicon devices is basically an extension of the EPROM process with the addition of an extra polysilicon layer. The three polysilicon layers are vertically integrated, which results in a compact cell layout that is about a factor of two smaller than a FLOTOX cell for a given generation of technology. This gives them an edge over the FLOTOX devices for memories larger than 256 kb. However, the textured-polysilicon memory requires higher operating voltage (> 20 V) to support its operation. The dominant failure mechanism in a textured poly cell is electron trapping, which results in a memory window closure [66].

3.5.2 EEPROM Architectures

The advances in EEPROM technology have enabled the scaling of these devices from the older 16 and 64 kb levels to 256 kb and multimegabit generation. For high-density EEPROMs, the cell size is the most critical element in determining the die size, and hence the manufacturing yield. For given program/erase threshold performance requirements, the scaling of an EEPROM cell usually requires a thinner dielectric. However, a thinner dielectric may result in higher infant mortality failures and a lower cell endurance life cycle. The oxynitride films of 90–100 Å thickness for the EEPROM cells have proven to be quite reliable because of their low charge trapping, lower defect density, and higher endurance characteristics. An n-well double-polysilicon gate CMOS technology was developed by SEEQ Technology, Inc., that uses oxynitride film 70–90 Å thick to produce a 54 μm^2 cell size for a 256 kb density EEPROM [67]. This cell has been shown to operate with a programming voltage as low as 17 V, and programming times as short as 0.1 ms. The endurance characteristics of this device (Q-cell design) are specified as over 1 million cycles/byte.

Figure 3-29(a) shows the Q-cell floating-gate memory transistor cross-section [68]. The SEEQ EEPROM memory cell consists of a floating-gate memory transistor and a select transistor, as shown in the schematic of Figure 3-29(b). The select transistor is used to isolate the memory transistor to prevent data disturb. The other peripheral logic is combined to form the Q-cell which incorporates the memory error-correction technique transparent to the user. The memory cell defines the logic states as either a "1" or a "0" by storing a negative or a positive charge on the floating gate (Poly 1). When the reference voltage is applied to the top control gate (Poly 2), the addressed memory cell will either conduct or not conduct a current. This cell current is detected by the sense amplifier and transmitted to the output buffers as the appropriate logic state.

The charge is transferred to and from the floating gate through the Fowler–Nordheim tunneling process, as explained earlier. The tunneling occurs when a high voltage (typically 17–20 V) is placed across the tunnel dielectric region of the memory cell. This high voltage is generated internally, on-chip. For a logic "1," the electrons are stored on the floating gate, using the conditions defined for the "erase" operation. For a logic "0," the holes are stored on the floating gate, using the conditions defined for a "write" operation. The Q-cell thresholds for a logic "1" and "0" are shown in Figure 3-29(c) [68].

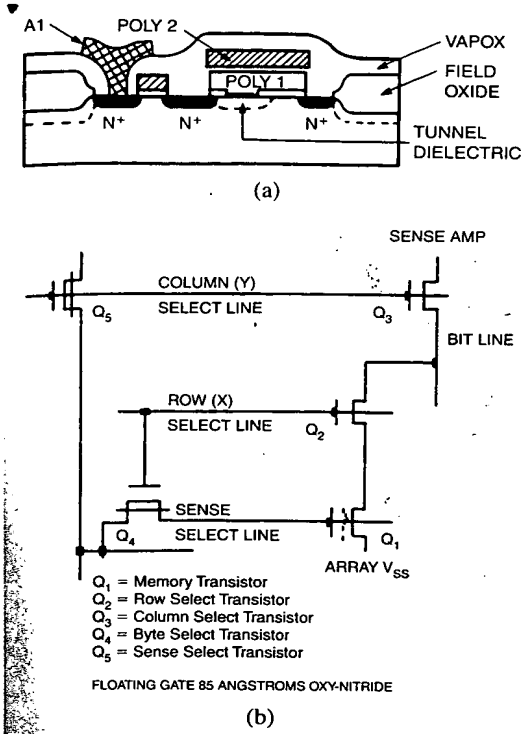


Figure 3-29. SEEQ EEPROM "Q-cell." (a) Floating-gate transistor cross-section. (b) Memory cell schematic. (c) Cell margin characteristics. (From [68], with permission of SEEQ Technology, Inc.)

For 256 kb EEPROMs, JEDEC Standard requires some standard features, such as: operation with a primary power supply voltage of 5 V, input levels between 0 and 5 V, read and write timing cycles consistent with the standard timing diagrams, operation in conformance with the standard truth table, etc. [69]. This standard also defines the implementation protocols and requirements for some optional features, including the page write mode, DATA-polling, software data protection, and write protect.

An example is the ATMEL 256 kb CMOS EEPROM organized as 32,768 words × 8 b, and offers a read access time of 70 ns, an active current of 80 mA, and a standby current of 3 mA [70]. Figure 3-30(a) shows the pin configurations and block diagram of this device which is accessed like a RAM for the read or write cycle without the need for any external components. It contains a 64 byte page register to allow for writing up to 64 bytes simultaneously using the page write mode. During a write cycle, the address and 1–64 bytes of data are internally latched, which frees the addresses and data bus for other operations. Following the initiation of a write cycle, the device automatically writes the latched data using an internal control timer. The end of a write cycle can be detected by DATA-polling of the I/O7 pin. Once the end of a write cycle has been detected, a new access for read or write can begin. In addition to the DATA-polling, there is another method for determining the end of the write cycle. During a write operation, successive attempts to read data from the device will result in I/O6 toggling between 1 and 0. However, once the write operation is over, I/O6 will stop toggling and valid data will be read. Figure 3-30(b) shows the AC Read waveforms, and (c) shows the Page Mode Write waveforms.

A hardware data protection feature protects against inadvertent writes. An optional software-controlled data protection feature is also available and is user-controlled. Once it is enabled, a software algorithm must be issued to the device before a write operation can be performed. This device utilizes internal error correction for the extended endurance and improved data-retention characteristics. The endurance is specified at 10^4 or 10^5 cycles, and the data retention at ten years.

A 1 Mb EEPROM using dual-gate MONOS (metal–oxide–nitride–oxide–semiconductor)